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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
FENTY, JESSE A

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,171	KER ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *18-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun et al. (U.S. Patent No. 6,406,948 B1).

In re claim 1, Jun discloses an ESD protection circuit with low input capacitance (stacked diodes), suitable for an I/0 pad, comprising a plurality of diodes (Fig. 10), stacked and coupled between a first power line (V_{DD}) and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between a second power line (V_{SS}) and the I/O pad, the diodes are forward-biased to conduct ESD current.

In re claim 13, Jun (Fig. 9) discloses the device of claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain (14) and substrate (P-type) of a MOS.

In re claim 14, Jun discloses the device of claim 13, but does not expressly disclose the gate electrodes connected to power lines. However, one skilled in the art will recognize that gate electrodes being connected to power lines are a necessary condition for any MOS type device to

work. That the gate electrodes of Jun, if not specifically mentioned, are connected to power lines is inherent.

In re claims 16 and 17, Jun discloses MOS transistors but does not expressly disclose the conductivity of the transistors. Those skilled in the art will recognize the interchangeability of the two types of devices and will recognize the suitability of selecting either an NMOS or PMOS configuration to be determined by the suitability of the intended use of the claimed device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (as above).

In re claim 2, Jun discloses the device of claim 1, wherein each diode is a PN junction diode formed by placing a doped area of a first conductivity type in a first well (16) of a second conductivity type, a deep well (12) of the first conductivity type formed under the first well to isolate the first well from a substrate (10) of the second conductivity type.

Jun does not expressly disclose a doped area a first conductivity type in the first well (16). However, it would have been obvious for one skilled in the art at the time the invention was made to insert such a region for the purpose of increasing the threshold voltage of the ESD device.

In re claim 3, Jun discloses the device of claim 2, wherein the first well (16) is surrounded by a second well (12) of the first conductivity type.

In re claim 4, Jun discloses the device of claim 2, wherein the first conductivity type is N type and the second conductivity type is P type.

5. Claims 5-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun as applied to claim 1 above, and further in view of Watt (U.S. Patent No. 5,623,156).

In re claim 5, Jun discloses the device of claim 1, but does not expressly disclose an ESD clamp. Watt discloses an ESD clamp circuit (24). It would have been obvious for one skilled in the art at the time of the invention to use as ESD clamp circuit as disclosed by Watt for the device of Jun for the purpose, for example, of enhancing ESD protection to the internal circuit.

In re claim 6, Jun in view of Watt discloses the device of claim 5, wherein the power-rail ESD clamp circuit includes a substrate triggered MOS including two source/drains (34, 36) coupled to the first power line and the second power line respectively, the substrate node biased with suitable current to trigger a BJT (44_1) parasitizing in the substrate-triggered MOS, and conducting ESD current when an ESD event occurs.

In re claim 7, Jun in view of Watt discloses the device of claim 6, wherein the substrate-triggered MOS includes a gate applied with a bias voltage. The limitation, "to keep the substrate ... operations" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 8 Jun in view of Watt discloses the device of claim 6, wherein the gate is applied with a bias voltage. The limitation, "to speed up ... occurs" is a recitation of the intended use of the claimed invention and without a more defining structural limitation, is not given patentable weight as to the structure of the device.

In re claim 9, Jun in view of Watt discloses the device of claim 6, but does not expressly disclose the substrate-triggered MOS formed in a first well of a first conductivity type surrounded by a second well of the second conductivity type. However, it would have been obvious for one skilled in the art at the time the invention was made to for the MOS device in wells of this type because it is well known in the art to place transistor devices in doped well for the purpose, for example, of providing better device isolation as compared to simply forming the devices in the substrate, where they may be susceptible to back surface stray currents and voltages.

In re claim 10, Jun in view of Watt discloses the device of claim 9, wherein the first well is surrounded by a second well of the first conductivity type.

In re claim 11, Jun in view of Watt discloses the device of claim 5, wherein the power-rail ESD clamp circuit includes an ESD detection circuit to detect the occurrence of the ESD event.

In re claim 12, Jun discloses the device of claim 1, but does not expressly disclose a MOS diode. Watt discloses a MOS diode (20). It would have been obvious to one skilled in the art at the time the invention was made to utilize an additional diode in the form of a MOS diode as disclosed by Watt for the purpose, for example, of providing secondary ESD protection (Watt; column 8, lines 30-33).

In re claim 15, Jun discloses the device of claim 13, but does not expressly disclose the gate of the MOS couples to a second source/drain of the MOS. Watt discloses the configuration of the gate of a MOS being coupled to the source/drain of a MOS. It would have been obvious to one skilled in the art at the time the invention was made to utilize an additional diode in the form of a MOS diode as disclosed by Watt for the purpose, for example, of providing secondary ESD protection (Watt; column 8, lines 30-33).

Response to Arguments

6. Applicant's arguments filed 05/12/03 have been fully considered but they are not persuasive.

Applicant argues that the stacked-diode device represented in Figure 10 is not described in the reference adequately to anticipate the claimed stacked-diode device. Jun's description that the diodes are large-area diodes is not dispositive of Figure 10 not reading the claimed invention. Jun discloses the devices being suitable for ESD protection, as claimed in the instant application.

Applicant concludes that there are no stacked diodes in Figure 9, contrary to the drawing in Figure 10. However, examiner cannot deviate from what is disclosed in the prior art. Prior art comprises all the components of a patent, including the drawings, specification and abstract. That one section of the patent does not appear to explain another section does not preclude the latter section from being reasonably relied upon in patent prosecution.

Regarding the rejections under 35 USC §103, motivations for adding a deep well to the device of Jun are provided in the rejection. Multiple well structures are well-known in the art.

Secondly, motivation is also provided for combining similar structured Jun and Watt references to make up for the deficiencies of the Jun reference. Motivation to combine references can come from the lead reference, the secondary reference, or from the knowledge of an ordinary worker in the art. In this case, ESD protection through the use of diodes is the shared purpose of the inventions. To enhance the stacked-diode structure of Jun with the clamp structure of Watt (Fig. 5) which discloses stacked diodes in parallel with ESD clamp structures would have been obvious to one of ordinary skill at the time the invention was made for the purpose of enhancing ESD protection.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty
Examiner
Art Unit 2815

JAF
July 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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